REMARKS

Applicant concurrently files herewith a Petition and fee for a One-month Extension of Time.

Claims 1-27 are all the claims presently pending in the application. Claims 1-7, 11, 15 and 17 have been amended to more particularly define the invention. Claims 19-27 have been withdrawn from prosecution. Of the remaining claims, claims 1, 14-15 and 17 are independent.

Attached hereto is a marked-up version of the changes made to the claims by the current Amendment. The attached page is captioned "**Version with markings to show changes made.**" These amendments are made only to more particularly point out the invention for the Examiner and not for narrowing the scope of the claims or for any reason related to a statutory requirement for patentability.

Applicant also notes that, notwithstanding any claim amendments herein or later during prosecution, that Applicant's intent is to encompass equivalents of all claim elements.

Claims 1-10 and 14-18 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Nishizawa, et al. (U.S. Patent No. 4,939,571). Claims 1-2, 6, and 14-18 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Ma, et al. (U.S. Patent No. 6,407,435).

These rejections are respectfully traversed in the following discussion.

I. THE CLAIMED INVENTION

The claimed invention is directed to a field effect transistor that includes a substrate, an insulating layer and a gate electrode. The substrate includes a source region, a drain region, and a

channel. The insulating layer is disposed over the channel region and includes a layer of aluminum nitride and at least one of aluminum oxide, silicon dioxide and silicon nitride disposed over the channel region. The gate electrode is disposed over the insulating layer.

Conventional high dielectric constant gate dielectrics for silicon complementary metal oxide semiconductor (CMOS) devices, such as transistors, use a silicon dioxide gate dielectric or silicon oxynitride. As CMOS devices miniaturize, scaling laws require that the ratio of permittivity and thickness of the dielectric layer also reduce. However, when the layer is below a thickness of 1.5 - 1.7 nanometers, the layer starts transmitting an unacceptably high amount of leakage current. Additionally, as the layer gets so thin, it also becomes impervious to the diffusion of impurities, or dopant atoms. Therefore, the dielectric layer fails to protect the underlying silicon substrate.

By contrast, the present invention includes an insulating layer that has a layer of aluminum nitride and at least one of aluminum oxide, silicon dioxide, and silicon nitride. In this manner, the present invention provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with Silicon dioxide whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

II. THE 35 U.S.C. § 112 SECOND PARAGRAPH REJECTION

The Examiner alleges that claims 11-13 are indefinite. While Applicant submits that such would be clear to one of ordinary skill in the art taking the present Application as a whole, to speed prosecution claim 11 has been amended. Specifically, Applicant notes that claim 11 has been amended to recite aluminum "nitride" rather than aluminum "oxide."

In view of the foregoing, the Examiner is respectfully requested to withdraw this rejection.

III. THE PRIOR ART REJECTIONS

The Examiner alleges that any one of the Nishizawa et al. reference and the Ma et al. reference teaches the claimed invention. Applicant submits, however, that there are elements of the claimed invention which are neither taught nor suggested by these references.

The Nishizawa et al. reference discloses an insulated-gate type transistor. In particular, the Nishizawa et al. reference discloses an insulating layer 6 with silicon dioxide, aluminum oxide, silicon nitride or aluminum nitride (Fig. 1, col. 2, lines 9-10; and col. 3, lines 37 - 39). The Nishizawa et al. reference does not teach or suggest the features of independent claims 1, 14-15 and 17 including a layer of aluminum nitride and at least one of aluminum oxide, silicon dioxide, and silicon nitride.

In particular, the Nishizawa et al. reference does not recognize the benefits that the aluminum nitride layer has over conventional silicon dioxide. As evidenced by the listing in the Nishizawa et al. reference at col. 2, lines 9-10, appears to disclose that silicon dioxide and

aluminum nitride are interchangeable. Clearly, the Nishizawa et al. reference does not teach or suggest the advantages of the present invention.

As explained above, the aluminum nitride is important because it provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with Silicon dioxide whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

The Nishizawa et al. reference does not teach or suggest these advantages and therefore does not teach or suggest the features of the independent claims including a layer of aluminum nitride and at least one of aluminum oxide, silicon dioxide and silicon nitride.

The Ma et al. reference also does not teach or suggest the features of the present invention. The Ma et al. reference discloses a multilayer dielectric stack and method of producing that stack. The Ma et al. reference discloses a multilayer dielectric stack 116 which includes an interposing layer 130 between a high dielectric layer 140 and the silicon substrate 112 (Fig. 2). In a manner similar to the Nishizawa et al. reference, the Ma et al. reference discloses that the interposing layer 130 may include aluminum oxide, aluminum nitride, silicon nitride or silicon dioxide (col. 1, lines 64-67).

In particular, the Ma et al. reference does not recognize the benefits that the aluminum nitride layer has over conventional silicon dioxide. As evidenced by the listing in the Ma et al. reference at col. 1, lines 64-67, appears to disclose that silicon dioxide and aluminum nitride are interchangeable. Clearly, the Ma et al. reference does not teach or suggest the advantages of the present invention.

As explained above, the aluminum nitride is important because it provides a high dielectric constant gate dielectric for a CMOS transistor. In comparison with Silicon dioxide whose permittivity is restricted to a minimum of 3.8, the permittivity of aluminum nitride is in the range of approximately 9 - 16. As a result, the physical thickness can be as much as 2.5 times higher than silicon dioxide and yet still maintain the same e/d ratio. Therefore, as a result of the capability of having greater thickness, the aluminum nitride layer will conduct a far lower leakage current than the silicon dioxide layer and will also protect much better against the diffusion of impurities and dopants and will better protect the underlying silicon substrate.

The Ma et al. reference does not teach or suggest these advantages and therefore does not teach or suggest the features of the independent claims including a layer of aluminum nitride and at least one of aluminum oxide, silicon dioxide and silicon nitride.

IV. FORMAL MATTERS AND CONCLUSION

In view of the foregoing amendments and remarks, Applicant respectfully submits that claims 1-27, all the claims presently pending in the Application, are patentably distinct over the prior art of record and are in condition for allowance. The Examiner is respectfully requested to

pass the above application to issue at the earliest possible time.

Should the Examiner find the Application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary in a telephonic or personal interview.

The Commissioner is hereby authorized to charge any deficiency in fees or to credit any overpayment in fees to Assignee's Deposit Account No. 50-0510.

Respectfully Submitted,

Date: 11/4/02

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VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the claims:

Please amend claims 1-7, 11, 15 and 17 as follows:

1. (Amended) A field effect transistor, comprising:

a substrate comprising a source region, a drain region, and a channel region therebetween;

an insulating layer disposed over said channel region, said insulating layer comprising a layer comprising aluminum nitride and at least one of a layer of aluminum oxide, a layer of silicon dioxide, and a layer of silicon nitride disposed over said channel region; and

a gate electrode disposed over said insulating layer.

2. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of aluminum oxide is disposed upon said channel region, said aluminum nitride disposed over said aluminum oxide.

3. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of aluminum oxide is disposed over said channel region, said aluminum nitride disposed under said aluminum oxide.

4. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of silicon dioxide is disposed upon said channel region, said aluminum nitride disposed over said silicon dioxide.

5. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of silicon dioxide is disposed over said channel region, said aluminum nitride disposed under said silicon dioxide.

6. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of silicon nitride is disposed upon said channel region, said aluminum nitride disposed over said silicon nitride.

7. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of silicon nitride is disposed over said channel region, said aluminum nitride disposed under said silicon nitride.

11. (Amended) The transistor of claim 1, wherein said [insulating layer further comprises:

a] layer of aluminum oxide is disposed over said aluminum [oxide] nitride.

15. (Amended) A semiconductor device, comprising:

a substrate comprising a source region, a drain region, and a channel region therebetween;

an insulating layer disposed over said channel region, said insulating layer comprising a layer comprising aluminum nitride and at least one of aluminum oxide, silicon dioxide, and silicon nitride disposed over said channel region; and

a gate electrode disposed over said insulating layer.

17. (Amended) A multi-terminal device, comprising:

a substrate comprising a source region, a drain region, and a channel region therebetween;

an insulating layer disposed over said channel region, said insulating layer comprising a layer comprising aluminum nitride and at least one of aluminum oxide, silicon dioxide, and silicon nitride disposed over said channel region; and

a gate electrode disposed over said insulating layer.